converting the timing discrete analog signal levels to corresponding timing digital signals in response to the clock signals, and wherein the shifting further comprises shifting the phase of the clock signals in response to the timing digital signals.

B7 Cont'd.

213. (New) The method of claim 212 wherein the shifting comprises shifting the phase of the clock signals in response to both the timing digital signals and the digital information signals.

REMARKS

Support for the amendments to claims 145, 151 and 163 is found, for example, in the embodiments described in the Abstract, lines 4-8, on page 3, lines 25-33, page 5, lines 50-53, page 7, lines 15-19 and 45-50; page 8, lines 39-43; and page 9, lines 40-45 of the specification.

New claims 167-213 have been added to more fully protect the invention.

The claims are believed to be in compliance with the recapture rule, MPEP § 1412.02. Regarding, for example, new claims 192-213, see *Mentor Corp. v. Coloplast, Inc.*, 998 F.2d 992, 994, 27 USPQ2d 1521, 1525 (Fed. Cir. 1993) cited in § 1412.02 (8th Ed., p. 1400-15).

Support for new claims 167 and 176 is found, for example, in the embodiments described in the Abstract, lines 4-8, on page 3, lines 25-33, on page 7, lines 15-19 and 45-50; page 8, lines 39-43; page 9, lines 29-45; page 10, lines 11-6 and page 13, lines 55-67 of the specification.

Support for new claims 173-174, 179-180, 185-186, and 188-189 is found, for example, in the embodiments described on page 6, lines 41-52, page 10 lines 11-35, page 12, lines 1-10 and page 13 lines 55-67.

Support for new claims 192-213 is found, for example, in the embodiments described in connection with Figs. 3-7 and 11 and the related text found at page 5, line 37 – page 10, lines 35.

An information disclosure statement is submitted with this Amendment.

Responding to paragraph 1 of the Office Action, a copy of the Assignee's Assent dated March 15, 2000, submitted in connection with the parent reissue application is enclosed with this Amendment.

Responding to paragraph 2 of the Office Action, the applicants submit the Response dated February 9, 2001, submitted in connection with the parent reissue application. As stated in paragraph 1 of the Response, the original patent was hand delivered to the Examiner on January 26, 2001.

Responding to paragraph 3 of the Office Action, the reissue claims 145-166 are resubmitted in a second attachment in underlined form, as requested by the Examiner.

Responding to paragraphs 4-5 of the Office Action, the rejection of claims 145-147, 157-159, 163 and 166 under 35 U.S.C. 102(b) as being anticipated by Motley et al. (U.S. Patent No. 3,962,637, "Motley") is respectfully traversed. Amended claim 145 reads as follows (emphasis supplied):

145. (Amended) An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a plurality of analog levels defining information signals comprising:

an analog to digital converter arranged to convert the plurality of analog levels to corresponding digital information signals at a particular rate;

a timing recovery circuit arranged to regulate the particular rate at which said analog to digital converter converts the plurality of analog levels to the corresponding digital information signals; and

a digital adaptive equalizer arranged to identify one of the digital information signals with a level corresponding most closely to one of the plurality of analog levels defining information signals.

The digital adaptive equalizer limitation has been amended in a manner analogous to the amendment of original claims 1 and 14 in order to bring the claim into compliance with the recapture rule, MPEP § 1412.02.

Regarding the Examiner's statement that Motley teaches an A/D converter 67 for converting data symbols, Col. 5, lines 10-16 of Motley state:

> Each of the data sumbols [sic.]... expresses one of a plurality of data levels, the number of which depends on the speed of operation. For 4800 bps operation, the symbols will typically express one of three levels (such as .+-.1.732,0) in one of the I and Q channels, and one of five levels (such as .+-.2,.+-.1,0) in the other of the I and Q channels.

According to Col. 5, lines 33-4:

> After being appropriately filtered, the signals in the I and Q channels can be introduced to multipliers 42 and 44, respectively, wherein they are multiplied at a carrier frequency, such as 1600 Hertz, by digital quantities from a sine/cosine ROM 45. These modulated signals can then be combined in an adder 47, converted to analog format in a digital-to-

analog converter 49, and smoothed by an analog lowpass filter 51. In its analog format the signal is then introduced into the telephone lines 23.

Thus, the Motley telephone lines do not carry analog signals defining information signals as claimed. According to Col. 6, lines 30-61:

> The receiver 29 will typically receive the input analog signal from the telephone line 23 and will pass this signal through an analog filter 63 and an automatic gain control 65. The filter 63 identifies the desired passband, and the automatic gain control 65 provides the desired signal level. An analog-to-digital converter 67, which may include a sampler, is provided to sample and digitize the incoming analog signal at a rate, such as 6400 times per second, corresponding to some multiple of the symbol or baud rate of the transmitter 33.
>
> In a conventional manner the converter 67 is controlled by a timing signal which is characterized by a stream of clock pulses. The converter 67 responds to each of the pulses by taking a single sample of the analog signal and by expressing the amplitude of the sample as a digital number. The pulses in the timing signal are separated by a timing interval which can be adjusted to vary the sampling rate of the converter 67.
>
> It will be noted that in this embodiment the signals throughout the remainder of the receiver 29 have a digital format.
>
> The digital signals from the converter 67 can be separately multiplied in each of a pair of multipliers 69 and 71 by quantities from a

sine/cosine ROM 73. In this manner, the signal can be noncoherently demodulated and separated into an I channel and a Q channel in the receiver 29.

Thus, Motley does not identify analog signals defining information signals as claimed. In contrast to Motley, claim 1 includes a digital adaptive equalizer arranged to identify one of the digital information signals with a level corresponding most closely to one of the plurality of analog levels defining information signals. Motley does not teach or suggest such apparatus. No known part of the Motley modem identifies a digital information signal with a level corresponding most closely to one of a plurality of analog levels defining information signals as claimed. As explained in the parent patent (RE37,826) at Col. 2, lines 7-12, an equalizer of the type claimed is able to enhance the resolution provided by the equalizer in determining the amplitude level of the digital information signals. This is a feature that merits patent protection. Nothing like the claimed equalizer is taught or suggested by Motley. For all the foregoing reasons, claim 1 is allowable.

Claims 146 and 147 are dependent on claim 145 and are allowable for the same reasons as claim 145.

Claims 157-159 have been canceled.

Claim 163 has been amended in a manner analogous to claim 145 and is allowable for the same reasons as claim 145. Amended claim 166 is dependent on claim 163 and is allowable for the same reasons as claim 163.

Responding to paragraphs 6-7 of the Office Action, the rejection of claims 148, 154 and 160 under 35 U.S.C. 103(a) as being unpatentable over Motley in view of Loyer

(U.S. Patent No. 4,652,874, "Loyer") is respectfully traversed. Claim 148 is dependent on claim 145 and is allowable for the same reasons as claim 145. Claim 154 is dependent on claim 151 and is allowable for the same reasons as claim 151, which will described in response to paragraph 9 of the Office Action. Claim 160 has been canceled.

Responding to paragraph 8 of the Office Action, the rejection of claims 149, 155 and 161 under 35 U.S.C. 103(a) as being unpatentable over Motley in view of Wang et al. (U.S. Patent No. 5,052,000, "Wang") is respectfully traversed. Claim 149 is dependent on claim 145 and is allowable for the same reasons as claim 145. Wang does nothing to cure the deficiencies in the teaching of Motley. Wang does not transmit analog levels as claimed. Analog signals could not be used, because there is no digital to analog converter in the transmitter shown in Fig. 2 and no analog to digital converter in the receiver shown in Fig. 2. Thus, Wang does not and could not teach or suggest an equalizer which identifies a digital information signal with a level corresponding most closely to one of a plurality of analog levels defining information signals as claimed in claim 145. For the foregoing reasons, claim 149 is allowable.

Claim 155 is dependent on claim 151 and is allowable for the same reasons as claim 151, which will be explained in response to paragraph 9 of the Office Action.

Claim 165 is dependent on claim 163 and is allowable for the same reasons as claim 163 previously explained.

Responding to paragraph 9 of the Office Action, the rejection of claims 151-153 and 165 under 35 U.S.C. 103(a) as being unpatentable over Motley is respectfully

traversed. Claim 151 has been amended to depend on claim 145 and is allowable for the same reasons as claim 145.

Claims 152 and 153 have been canceled.

Claim 165 is dependent on claim 163 and is allowable for the same reasons as claim 163.

Responding to paragraph 10 of the Office Action, the allowability of claims 150, 156, 162 and 164 if rewritten in independent form is gratefully acknowledged. Claim 150 has been rewritten as new claim 188, claim 156 has been rewritten as new claim 189, claim 162 has been rewritten as new claim 190 and claim 164 has been rewritten as new claim 191

In summary, each of claims 145-151 and 163-194 is allowable, and such action is respectfully requested.

Date: May 28, 2003

Respectfully submitted,

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Version of Amended Specification and Claims With Markings To Show Changes Made
Case No. 13470US02
Serial No. 09/620,919

On page 1, in the CROSS REFERENCE TO RELATED APPLICATIONS submitted with the preliminary amendment, kindly delete the present paragraph and substitute the following paragraph:

This application is a continuation of [allowed] Application No. 09/252,551 filed February 18, 1999, now U.S. Reissue Patent No. RE37,826, which was a reissue of Patent No. 5,604,741 issued February 18, 1997, the disclosures of which are incorporated fully herein by reference.

145. (Amended) An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a [multi-level signal] plurality of analog levels defining information signals[,] comprising:

an analog to digital converter [for digitally converting] arranged to convert the [multi-level signal] plurality of analog levels to corresponding digital information signals at a particular rate;

a timing recovery circuit [for regulating] arranged to regulate the particular rate at which said analog to digital converter converts the [multi-level signal] plurality of analog levels to the corresponding digital information signals; and[,]

a digital adaptive equalizer [for receiving the digitally converted multi-level signal and selecting] arranged to identify one of [a plurality of levels] the digital information signals with a level corresponding most closely to one of the plurality of analog levels defining information signals.

150. (Amended) The apparatus of claim 145, wherein said timing recovery circuit regulates the particular rate in accordance with a product of a plurality of [peak] signal samples.

151. (Amended) [An] The apparatus of claim 145 wherein the at least one pair of twisted wires carry the multi-level signal at [that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal transmitted at] a transmission rate of at least 25 megasymbols per second[, comprising:

an analog to digital converter that is responsive to the multi-level signal transmitted at the transmission rate of at least 25 megasymbols per second;

a clock recovery circuit coupled to said analog to digital converter; and,

a digital adaptive equalizer coupled to said analog to digital converter].

163. (Amended) A method for recovering a [multi-level signal] plurality of analog levels defining information signals transmitted on at least one pair of twisted wires[,] comprising:

converting the [multi-level signal] plurality of analog levels defining information signals to [a] corresponding digital [signal] information signals at a particular rate;

regulating the particular rate of conversion;

[equalizing the digital signal;] and[,]

[selecting] identifying one of [a plurality of levels based on the digital signal] the digital information signals with a level corresponding most closely to one of the plurality of analog levels defining information signals.

164. (Amended) The method of claim 163, wherein the particular rate is regulated in accordance with a product of a plurality of [peak] signal samples.

166. (Amended) The method of claim 163, and further comprising decoding the identified [selected level] digital information signal.

Original Reissue Claims 145-166 Resubmitted In Underlined Form

Case No. 13470US02
Serial No. 09/620,919

145. An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal, comprising:

an analog to digital converter for digitally converting the multi-level signal at a particular rate;

a timing recovery circuit for regulating the particular rate at which said analog to digital converter converts the multi-level signal; and,

a digital adaptive equalizer for receiving the digitally converted multi-level signal and identifying one of a plurality of levels.

146. The apparatus of claim 145, further comprising an automatic gain control circuit coupled to said analog to digital converter.

147. The apparatus of claim 145, further comprising a decoder circuit coupled to said digital adaptive equalizer.

148. The apparatus of claim 147, further comprising a media access controller coupled to said decoder circuit.

149. The apparatus of claim 145, wherein said digital adaptive equalizer includes a feedforward equalizer, a data slicer and a decision feedback equalizer.

150. The apparatus of claim 145, wherein said timing recovery circuit regulates the particular rate in accordance with a product of a plurality of peak signal samples.

151. An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal transmitted at a transmission rate of at least 25 megasymbols per second, comprising:

an analog to digital converter that is responsive to the multi-level signal transmitted at the transmission rate of at least 25 megasymbols per second;

a clock recovery circuit coupled to said analog to digital converter; and,

a digital adaptive equalizer coupled to said analog to digital converter.

152. The apparatus of claim 151, further comprising an automatic gain control circuit coupled to said analog to digital converter.

153. The apparatus of claim 151, further comprising a decoder circuit coupled to said digital adaptive equalizer.

154. The apparatus of claim 153, further comprising a media access controller coupled to said decoder circuit.

155. The apparatus of claim 151, wherein said digital adaptive equalizer includes a feedforward equalizer, a data slicer and a decision feedback equalizer.

156. The apparatus of claim 151, wherein said timing recovery circuit regulates the particular rate in accordance with a product of a plurality of peak signal samples.

157. An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal, comprising:

an analog to digital converter;

a clock recovery circuit coupled to said analog to digital converter; and,

a digital adaptive equalizer coupled to said analog to digital converter.

158. The apparatus of claim 157, further comprising an automatic gain control circuit coupled to said analog to digital converter.

159. The apparatus of claim 157, further comprising a decoder circuit coupled to said digital adaptive equalizer.

160. The apparatus of claim 159, further comprising a media access controller coupled to said decoder circuit.

161. The apparatus of claim 157,wherein said digital adaptive equalizer includes a feedforward equalizer, a data slicer and a decision feedback equalizer.

162. The apparatus of claim 157, wherein said timing recovery circuit regulates the particular rate in accordance with a product of a plurality of peak signal samples.

163. A method for recovering a multi-level signal transmitted on at least one pair of twisted wires, comprising:

converting the multi-level signal to a digital signal at a particular rate;

regulating the particular rate of conversion;

equalizing the digital signal; and,

identifying one of a plurality of levels based on the digital signal.

164. The method of claim 163, wherein the particular rate is regulated in accordance with a product of a plurality of peak signal samples.

165. The method of claim 163, wherein the particular rate is at least 25 megasymbols per second.

166. The method of claim 163, decoding the identified level.